CLAIMS

1. A digitally configurable multiplexer/de-multiplexer, comprising:

a plurality of multiplexers, each receiving a plurality of address signals, selecting from among a plurality of first data signals, and coupling a selected first data signal to a corresponding one of a plurality of multiplexed signals;

a switch matrix having a first interface coupled to said plurality of multiplexed signals and a second interface coupled to a plurality of second data signals; and

configuration logic receiving a plurality of selection signals and coupled to control said switch matrix to couple selected ones of said plurality of multiplexed signals to said second interface.

2. The digitally configurable multiplexer/de-multiplexer of claim 1, wherein said plurality of multiplexers comprises M multiplexers, each receiving N address signals and coupling a selected one of 2^N first data signals to a corresponding one of M multiplexed signals in which N, M, Y = LOG_2M and N are positive integers, and wherein said configuration logic controls said switch matrix to configure said M multiplexers as a number $M/(2^{Y-X})$ of $(M/2^X)(2^N)$:1 multiplexer(s) in which X is a selected integer between 0 and Y.

3. The digitally configurable multiplexer/de-multiplexer of claim 2, wherein said plurality of multiplexers comprises four 8:1 multiplexers, each receiving three address signals and selecting from among eight first data signals and coupling a selected first data signal to a corresponding one of four multiplexed signals, and wherein said configuration logic configures said plurality of multiplexers as a selected one of four 8:1 multiplexers, two 16:1 multiplexers, and one 32:1 multiplexer.

4. The digitally configurable multiplexer/de-multiplexer of claim 1, wherein said switch matrix comprises an array of single-pole, single-throw (SPST) switches.

5. The digitally configurable multiplexer/de-multiplexer of claim 4, wherein said configuration logic comprises a first decoder receiving at least one configuration signal, a second decoder receiving at least one address signal, and digital logic coupled to said first and second decoders to control said array of SPST switches.

6. The digitally configurable multiplexer/de-multiplexer of claim 4, wherein said configuration logic comprises at least one register.

7. The digitally configurable multiplexer/de-multiplexer of claim 1, wherein said configuration logic comprises at least one register.

8. The digitally configurable multiplexer/de-multiplexer of claim 1, wherein said switching matrix comprises a cross-point matrix switch.

9. The digitally configurable multiplexer/de-multiplexer of claim 8, wherein said configuration logic comprises at least one register.

10. An integrated circuit (IC), comprising:

a first interface including a plurality of first analog signal lines;

a second interface including a plurality of second analog signal lines;

a third interface including a plurality of select signal lines;

a plurality of multiplexers, each having a plurality of data signal lines coupled to said first interface, a plurality of address inputs coupled to said third interface, and a corresponding one of a plurality of multiplexed signal lines;

a switch matrix, having a multiplexed interface coupled to said multiplexed signal lines and a data interface coupled to said second interface; and

configuration logic, having an input coupled to said third interface and an output coupled to control said switch matrix to couple selected multiplexed signal lines to said second interface.

11. The IC of claim 10, wherein said switch matrix comprises an array of single-pole, single-throw (SPST) switches.

12. The IC of claim 11, wherein said configuration logic comprises a first decoder receiving at least one configuration signal from said third interface, a second decoder receiving at least one address signal from said third interface, and digital logic coupled to said first and second decoders to control said array of SPST switches.

13. The IC of claim 10, wherein said configuration logic comprises at least one register programmable via said third interface.

14. The IC of claim 10, wherein said switching matrix comprises a cross-point matrix switch.

15. The IC of claim 14, wherein said configuration logic comprises at least one register programmable via said third interface.

16. A method of routing a plurality of analog signals, comprising:

distributing a plurality of first analog signals among a plurality of multiplexers;

selecting a configuration for the plurality of multiplexers;

addressing the plurality of multiplexers according to the selected configuration; and

coupling selected ones of a plurality of multiplexed signals from the plurality of multiplexers according to the selected configuration to a plurality of second analog data signals.

17. The method of claim 16, wherein said selecting a configuration comprises combining the plurality of multiplexers into groups.

18. The method of claim 17, wherein said addressing the plurality of multiplexers comprises routing a common set of address signals to each multiplexer of a group of multiplexers.

19. The method of claim 18, wherein said coupling selected ones of a plurality of multiplexed signals from the plurality of multiplexers comprises selecting a multiplexed signal of a multiplexer of a group of multiplexers.

20. The method of claim 19, wherein said selecting a multiplexed signal of a multiplexer of a group of multiplexers comprises selecting based on at least one address signal.